SPECIFICATION FOR LCM

韵唐光电

☐ Preliminary Specification
■ Final Specification

Customer Approve:

QC 品 质 ： _____

R&D 研 发 ： _____

Approved 批准： _____

产品型号(Description)： YT103IBLXL008-BS7-30

Compile by 编制	Quality/Engineer 品质/工程	Checked 审核	Approved 批准
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Table of contents

1.0 General Description.....4

2.0 Absolute Maximum Ratings.....5

3.0 Optical Characteristics.....6

4.0 Power On/Off Sequence.....9

5.0 Electrical Characteristics.....11

6.0 Reliability Test Items.....17

7.0 Interface Pin Connection.....18

8.0 Outline Dimension.....20

9.0 Package specification.....21

10.0 General Precaution.....22

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1.0 General description

1.1 Introduction

YT103IBLXL008-BS7-30 is model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 10.33 (7:16) inch diagonally measured active display area with WSVGA (720 horizontal by 1600 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.

1.2 Features

4 lanes MIPI Interface
Low driving voltage and low power consumption
ROHS Compliant

1.3 General information

Item		Specification	Unit	Remarks
Outline Dimension		115.3 x 251 x 4.63	mm	Tolerance:±0.2mm
Display area		106.92(W) x237.6(H)	mm	
Number of Pixel		720(H) x RGB x1600(V)	pixels	
Pixel pitch		0.0495(H) x 0.1485(V)	mm	
Pixel arrangement		Pixels RGB stripe arrangement		
Display mode		Normally Black		
Surface treatment		IPS Film		
Weight		TBD (Typ.)	gram	
Back-light		Single LED (Side-Light type)		
Driver IC	ICN	FL7705N		
Polarizer : zhuyou		Up: 0° sand surface Down 90° smooth surface	pcs	

1.4 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal(H)	115	115.3	115.6	mm
	Vertical(V)	250.7	251	251.3	mm
	Depth(D)	4.43	4.63	4.83	mm 不含柱子高度

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2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating (GND=AGND=0V)

Parameter	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage of Vdd	V_{DD}	-	-	V	
Power supply for Charge pump circuit	V_{SN}	-6.5	-6.5	V	
Power supply for Charge pump circuit	V_{SP}	4.5	6.5	V	
TFT Common Electrode Voltage	V_{COM}	-4	-0.3	V	

Note: (1) All of the Voltages listed above are with respective to GND=0V.
(2) Device is subject to be damaged permanently if stresses beyong those absolute maximum ratings listed above.

2.2 TFT LCD Power Supply Voltage

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	-	1.8V	-	V
	VSP	-	-	-	V
	VSN	-	-	-	V
	AVDD	9	10	13	V
VCOM	VCOM	-	-	-	V

Note: (1) VGH is TFT Gate operating voltage.
(2) VGL is TFT Gate operating voltage. The low voltage level of VGH signal must be fluctuates with same phase As Vcom.

2.3 Back-light Unit

Parameter	Symbol	Min	Typ	Max.	Unit	Note
LED Current	I_L	-	180	-	mA	Ta=25℃
LED Voltage	V_L	16.2	18	20	V	Ta=25℃
LED Life-time	h	20000	-	-	V	Ta=25 ℃ , If=25mA

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2.4 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Topa	-20	70	℃	
Storage Temperature	Tstg	-30	80	℃	

3.0 OPTICAL CHARACTERISTICS

3.1 Optical Specifications

Item	Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle range	Horizontal	θ L	CR > 10	80	85	--	Deg	Note (1,2)
		θ R		80	85			
	Vertical	θ U		80	85	--	Deg	
		θ D		80	85			
Luminance Contrast ratio		CR	θ = 0°	800	1000	--	--	Note (1,2)
Brightness		YL		350	400	--	Cd/cm2	Note (4,5)
Transmittance(pol)		T(%)	θ = 0°	--	5	--	%	
Color Gamut (C light)				--	70	--	%	
Reproduction of color （C-light）	White	Xw	θ =0°	-0.02	0.298	+0.03		Note (1,4)
		Yw			0.338			
	Red	Rx			0.663			
		Ry			0.320			
	Green	Gx			0.254			
		Gy			0.579			
	Blue	Bx			0.137			
		By			0.094			
Response Time (Rising + Falling)	Trt		Ta= 25° C θ = 0°	--	30	40	ms	Note (1,3)
Opetical View Direction			ALL					Note (1)

3.2 Measuring Condition

Measuring surrounding: dark room
Ambient temperature: 25±2℃
15min. warm-up time.

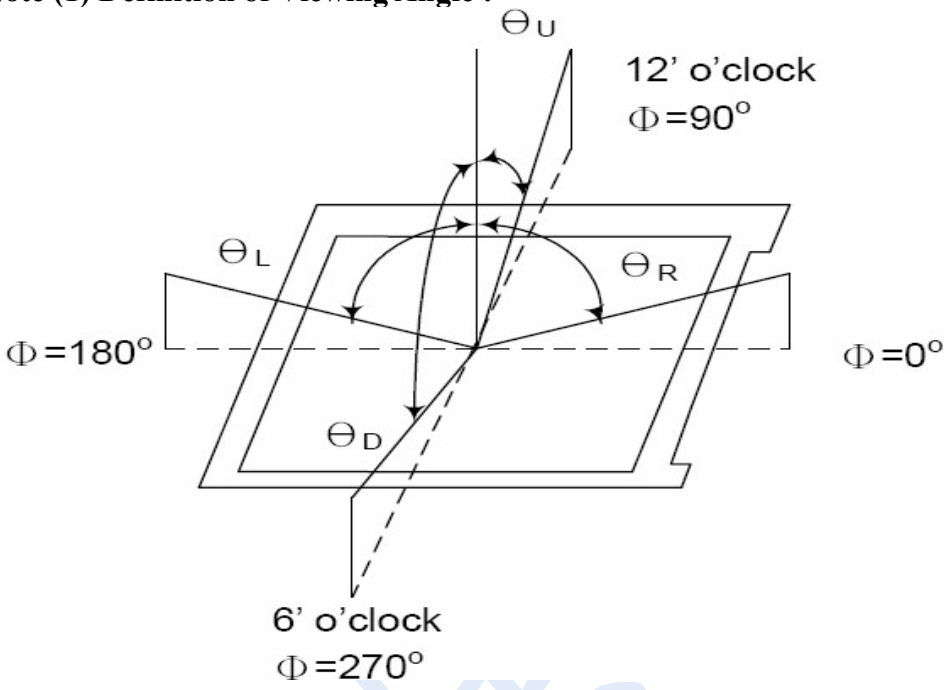
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3.3 Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-7 for other optical characteristics. Measuring spot size: 20 ~ 21 mm

Note (1) Definition of Viewing Angle :



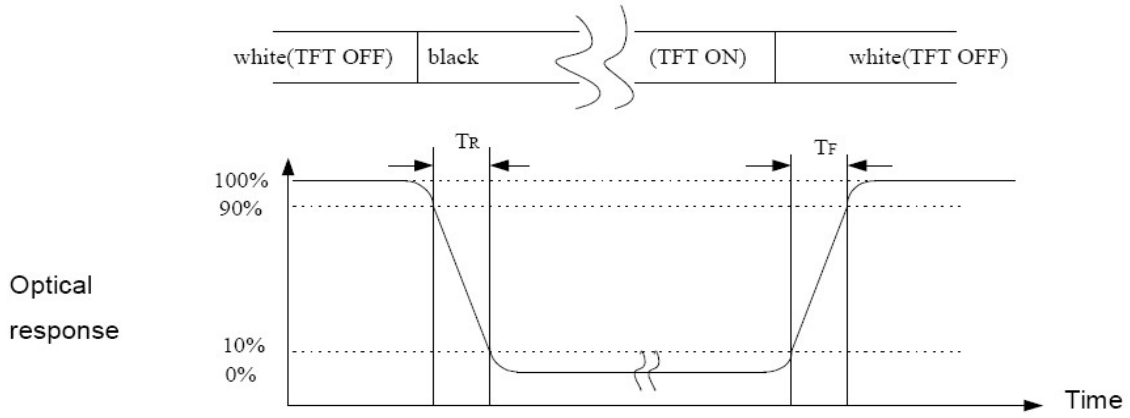
Note (2) Definition of Contrast Ratio (CR):
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

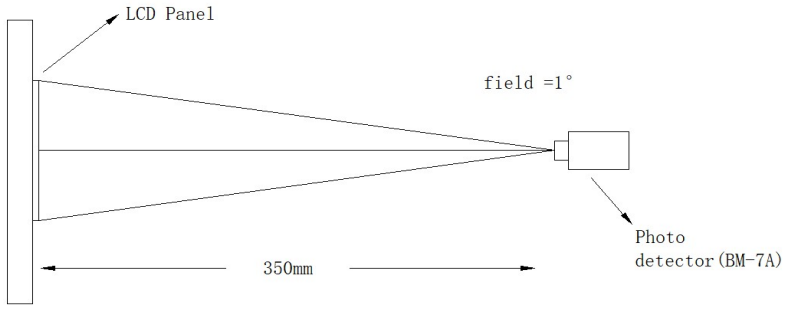
Note (3) Definition of Response Time: Sum of TR and TF

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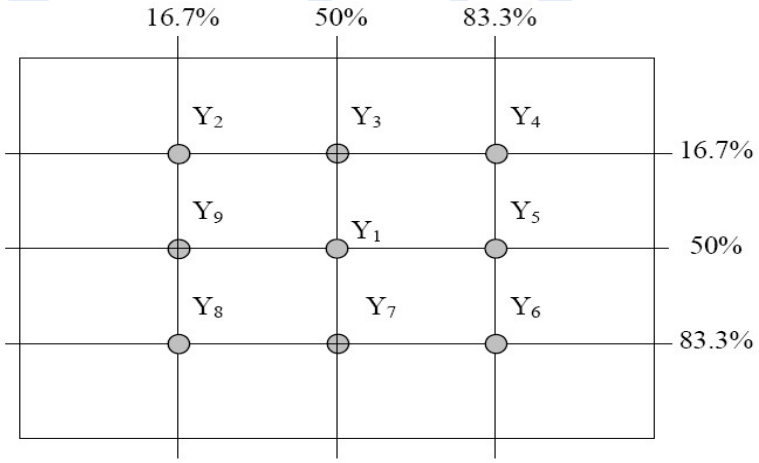
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Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity



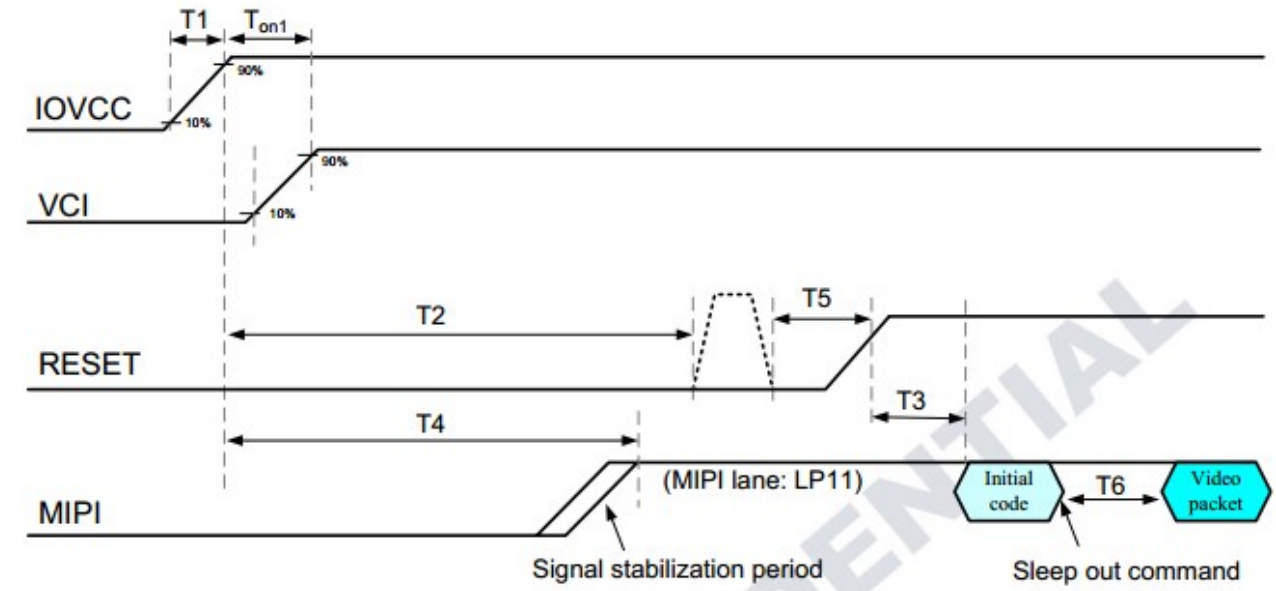
$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

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4.0 Power On/Off Sequence

To prevent the device damage from latch up,the power on/off sequence shown Below must be followed.

Applied Power: IOVCC, VCI



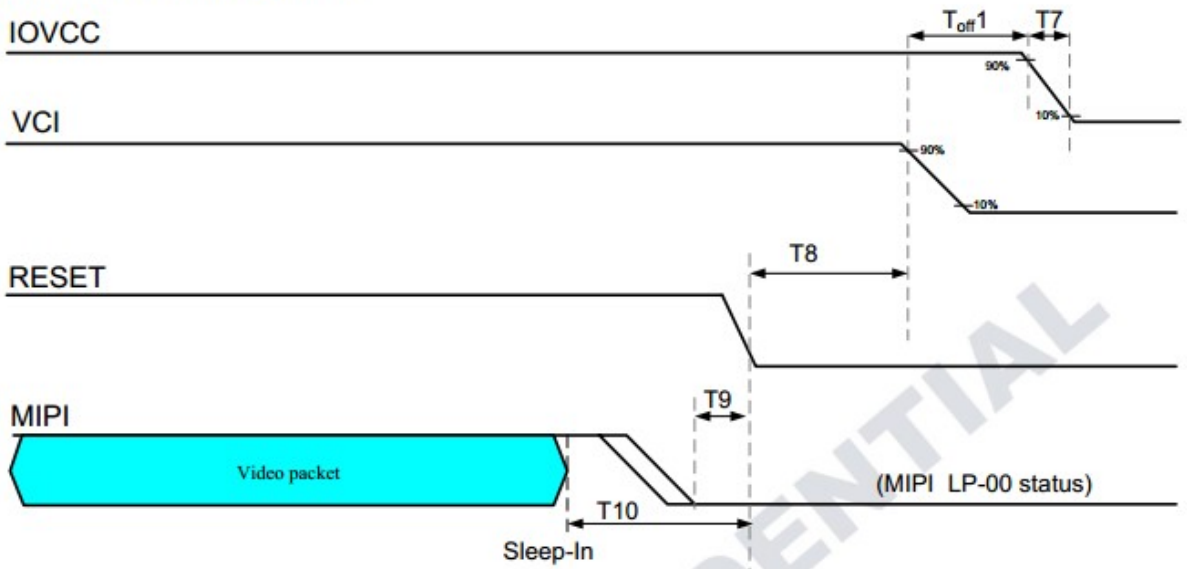
Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	Delay time of IOVCC to VCI	0			ms	
Ton2	Delay time of IOVCC to VSP	0			ms	
T1	IOVCC rising time	-		2	ms	
T2	Delay time of IOVCC to valid RESX to "H"	10			ms	
T3	Delay time of RESX "H" to initial code ready	20			ms	
T4	Delay time of IOVCC (HS_VCC) to MIPI bus ready	0		T2	ms	
T5	RESX "L" period	10			us	
T6	Delay time of initial code reloaded to video packet transmit	120			ms	

power on sequence timing

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Application Power: IOVCC, VCI,



Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Toff1	Delay time of VCI to IOVCC	0	-	-	ms	
Toff2	Delay time of VSP to IOVCC	0	-	-	ms	
Toff3	Delay time of VSN to VSP	0	-	-	ms	
T7	IOVCC falling time	-	-	-	ms	
T8	Delay time of RESX "L" to VCI	0	-	-	us	
T9	Delay time of MIPI LP-00 to valid RESX "L"	0	-	-	us	
T10	Delay time of Sleep-in received to valid RESX "L"	100	-	-	ms	
T11	Delay time of RESX "L" to VSN	0	-	-	ms	

power off sequence timing

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5.0 ELECTRICAL CHARACTERISTICS

5.1 DC Characteristics

Condition : Ta =25℃.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Power generation & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.6	3.0	3.6	V	1
Analog Operating voltage	VCI	Operating Voltage	4.5	5.5	6.5	V	2
Analog Operating voltage	VSP	Operating Voltage	4.5	5.5	6.5	V	
Analog Operating voltage	VSN	Operating Voltage	-6.5	-5.5	-4.5	V	
Analog Operating voltage	VCOM	Operating Voltage	-0.3	-	-4	V	
Analog Operating voltage	VGMP	Operating Voltage	3	4.5	6	V	
Analog Operating voltage	VGMN	Operating Voltage	-6	-4.5	-3	V	
Analog Operating voltage	|VGH-VGL|	Operating Voltage	|VGH-VGL| ≦30			V	
I/O operating voltage	IOVCC	I/O supply voltage	1.65	1.8	1.95	V	
MIPI Operating voltage	HS_VCC	HS-VCC supply voltage	1.1	1.2	1.3	V	
LOGIC INPUT/ OUTPUT							
Logic High level input voltage	VIH	-	0.7× IOVCC	-	IOVCC	V	3
Logic Low level input voltage	VIL	-	VSS	-	0.3× IOVCC	V	3
Logic High level output voltage	VOH	IOH = -0.1mA	0.8× IOVCC	-	IOVCC	V	4
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2× IOVCC	V	4
Logic High level leakage	ILIH1	Vin = 0 to IOVCC	-	-	1	μA	4,4
Logic Low level leakage	ILIL1	Vin = 0 to IOVCC	-1	-	-	μA	3,4
VCSW High level leakage	ILIH2	Vin = 0 to VCI	-	-	1	μA	5
VCSW Low level leakage	ILIL2	Vin = 0 to VCI	-1	-	-	μA	5
Source OP Output							
Output deviation voltage	V_{dev}	Sout≧4.2V Sout≦0.8V	-	-	30	mV	
Output deviation voltage	V_{dev}	4.2V>Sout>0.8V	-	-	20	mV	
Output offset voltage	V_{OFSET}	-	-	-	40	mv	
Stand-by Current							
Sleep In mode	I_{stlp}	DSI LP mode IOVCC Current	-	-	150	uA	
		DSI LP mode VSP Current	-	-	18	uA	2
		DSI LP mode VSN Current	-15	-	-	uA	2

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Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Ultra Low Power mode	I_{stul}	DSI Ultra Low power IOVCC Current	-	-	50	uA	
		DSI Ultra Low power VSP Current	-	-	18	uA	2
		DSI Ultra Low power VSN Current	-15	-	-	uA	2
Oscillator Output							
Oscillator tolerance	△OSC	Ta =25℃	-3%	-	3%	%	6

***Note* 1:** PCCS[1:0] pin = 10 mode.
***Note* 2:** PCCS[1:0] pin = 11 mode.
***Note* 3:** Including of RESX ,PCCS[1:0], BS[2:0], TEST_OSC, BIST, DCX, CSX, SCL, TEST[2:0].
***Note* 4:** Including of CABC_PWM_OUT, TE, TE_TOUCH.
***Note* 5:** Including of VCSW1, VSCW2.
***Note* 6:** Oscillator frequency= 58MHz.

DC Characteristics for DSI LP Mode

Condition : Ta =25℃,IOVCC =1.6V~3.6V, VCI =2.6V~3.6V.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0		200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK,D0)	880		1350	mV	
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK,D0)	0		550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0		300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.3	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Logic high level input voltage	I_{IH}	LP-RX,Vin =0~1.3V			10	uA	
Logic Low level input voltage	I_{IL}	LP-RX,Vin =0~1.3V	-10			uA	
Input pulse rejection	SGD	DSI-CLK+/-,DSI Dn+/-			300	Vps	1

Note 1: Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

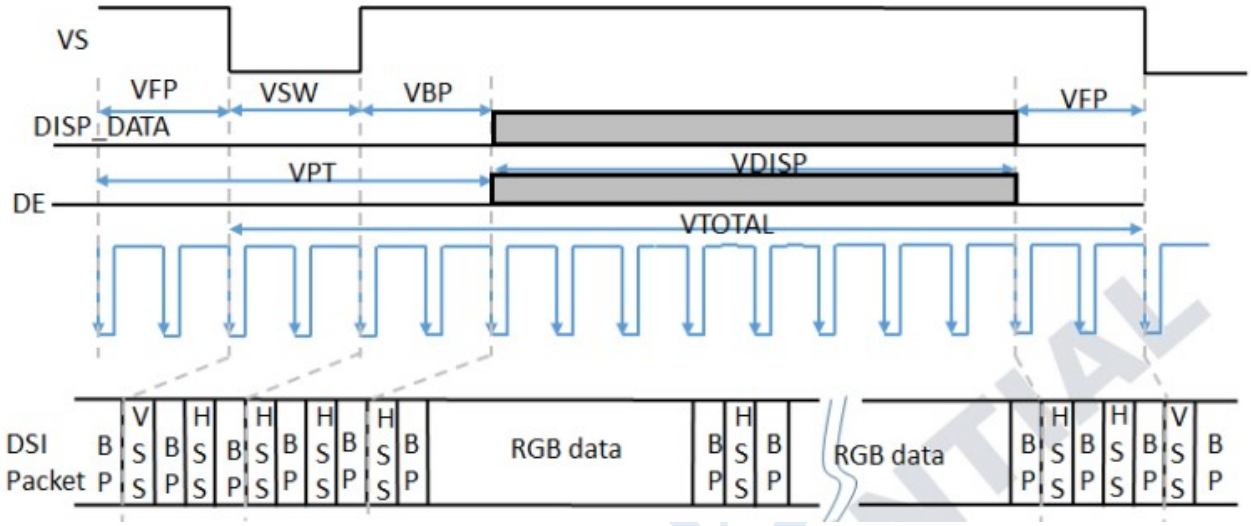


Spike/Glitch Rejection

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5.2 AC Characteristics

5.2.1 Vertical Timings for DSI video mode

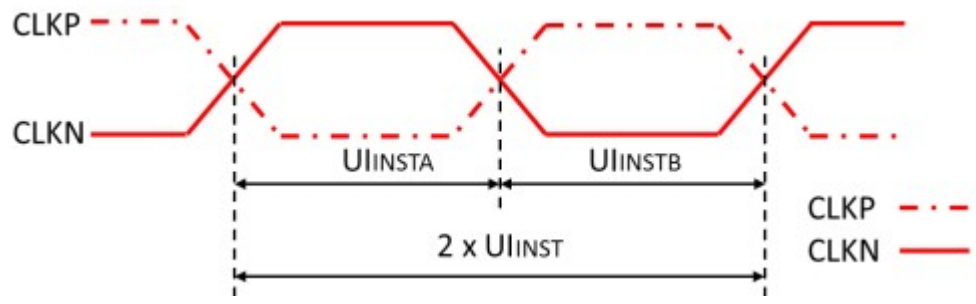


Condition : Ta =25℃,Resolution = 720(RGB)*1280.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
HS low pulse width	HSW		0.2			uS	
Horizontal back porch	HBP		1.0			uS	
Horizontal front porch	HFP		1.0			uS	
Horizontal data start point		HSW+HBP	1.2			uS	
Horizontal blanking period	HBLK	HSW+HBP+HFP	2.2			uS	
Horizontal active area	HDISP			-	720	DCLK	

5.2.2 MIPI AC Characteristic

- **High Speed Mode - Clock Timings**



Clock Timing

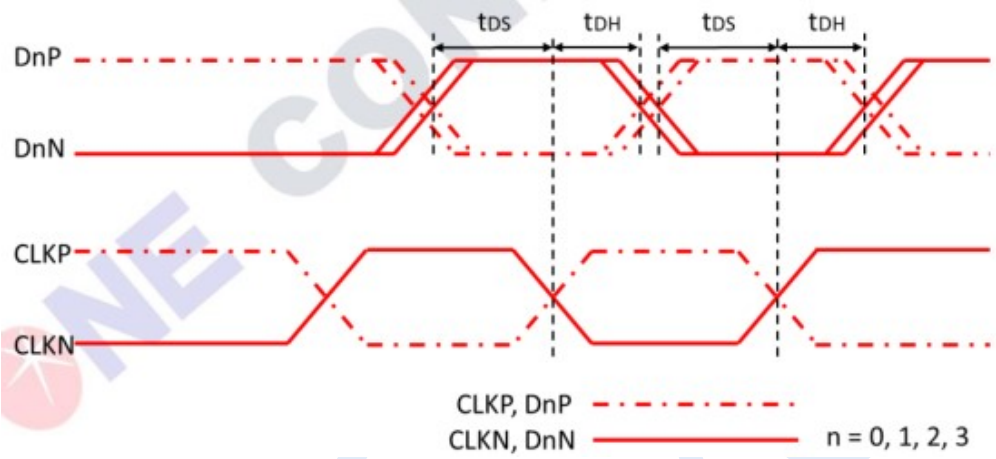
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Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	2.5		12.5	ns	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	1.25		6.25	ns	1,2

***Note** 1*: UI = UIINSTA = UIINSTB.

***Note** 2*: ICNL9707 can support max 600Mbps/lane at 4 lane and max 800Mbps/lane at 3 lane application.

- **High Speed Transmission**



DSI Clock / Data Timings

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

- **High Speed Clock Transmission**

After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM).

This sequence is illustrated below

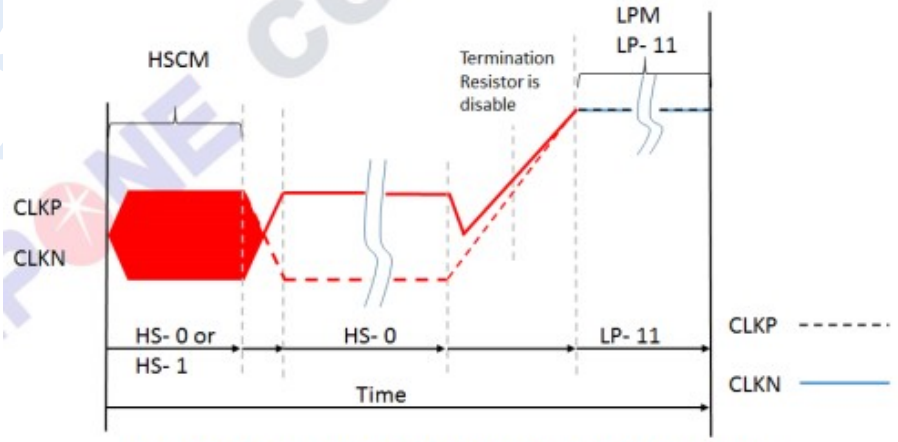
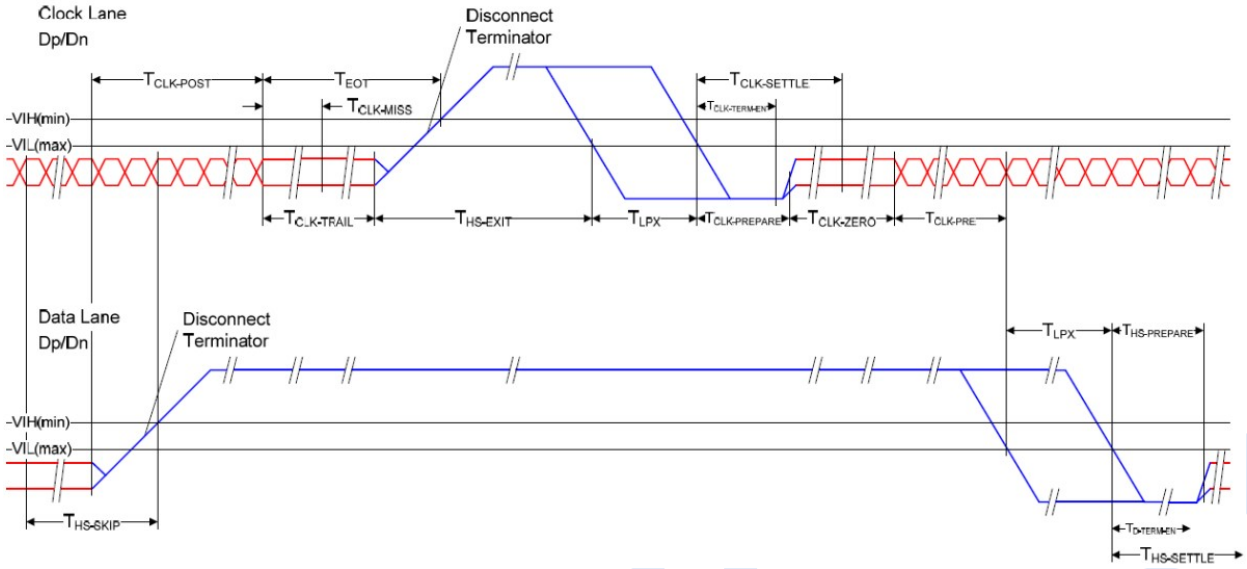


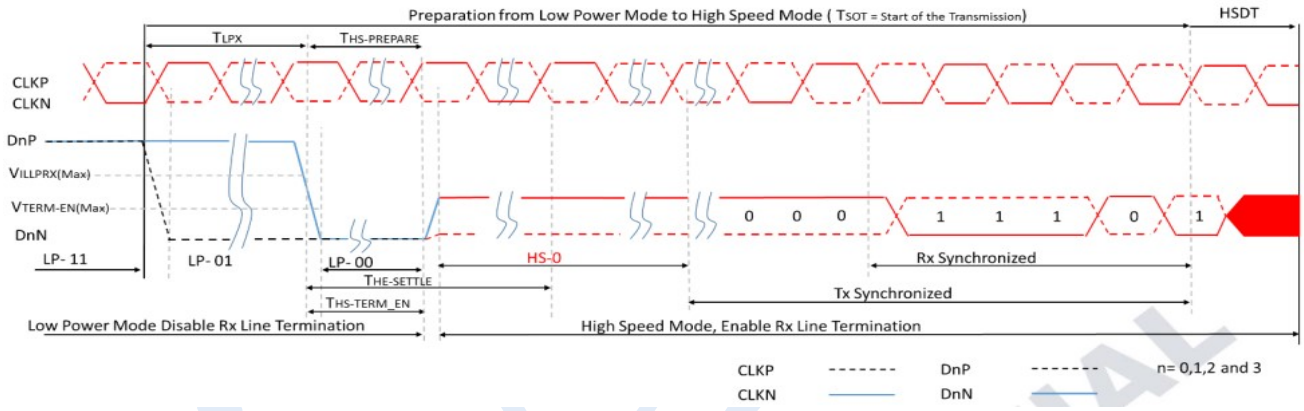
Figure 5-3 From High Speed Clock Mode (HSCM) to LPM

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- **Data Lanes from Low Power Mode to High Speed Mode**



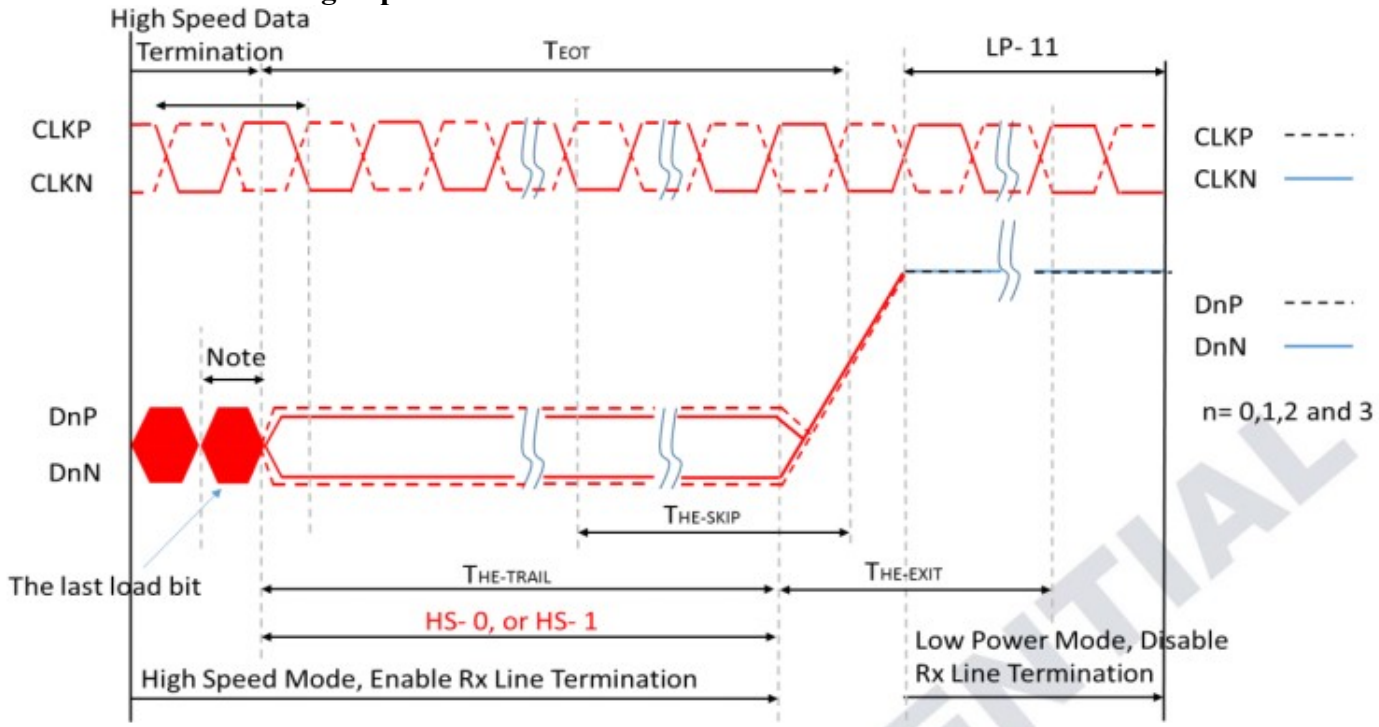
Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	TLPX	Length of any Low Power State Period	50			nS	1
DnP/N	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	THS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0,1,2 and 3.*

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- **Data Lanes from High Speed Mode to Low Power Mode**



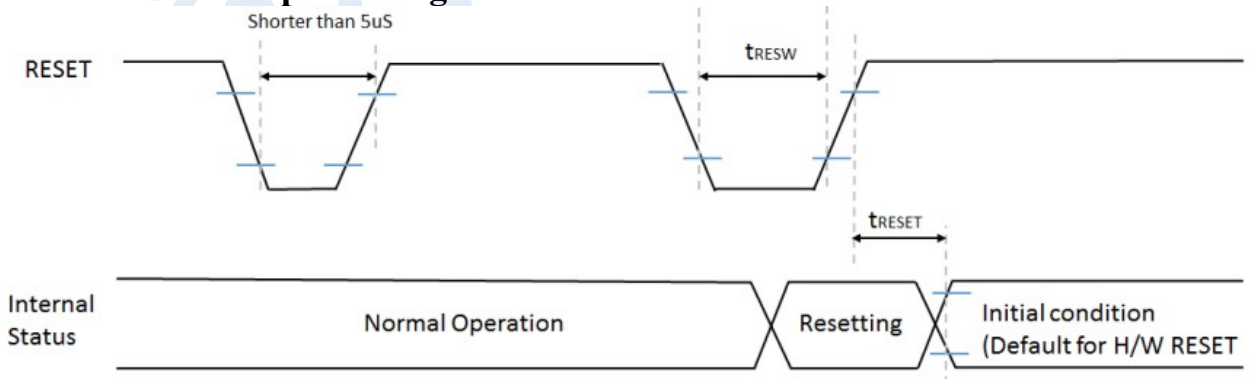
Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	THS-SKIP	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=*0,1,2 and 3.*

5.2.3 Reset Input timing table



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Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

***Note* 1:** Condition : Ta =25℃.

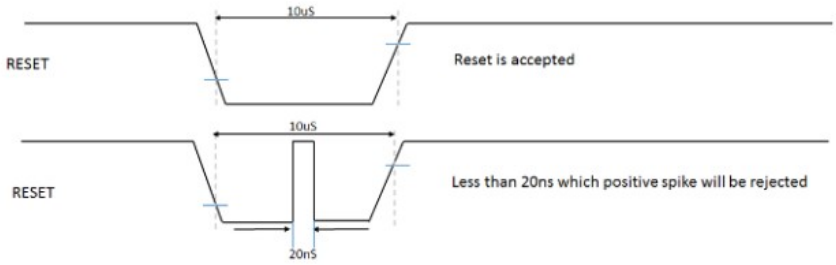
***Note* 2:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5us	Reset Rejected
More than 10uS	Reset
Between 5us and 10uS	Reset Start

***Note* 2:** During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

***Note 4*:** Spike Rejection also applies during a valid reset pulse as shown below:



***Note 5*:** It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

Horizontal timing

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Horizontal Display Area	thd		720		DCLK	
DCLK frequency	fclk	-	80	-	MHz	
HSD Period	th	-	800	-	DCLK	
HS pulse width	thpw	-	20	-	DCLK	
HS Back Porch(Blanking)	thbp		40		DCLK	
HS Front Porch	thfp	-	40	-	DCLK	

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Vertical timing

Parameter	Symbol	Min.	Typ.	Max	Unit	Note
Vertical Display Area	tvd		1600		TH	
VS period time	tv	-	1637	-	TH	
VS pulse width	tvpw	-	5	-	TH	
VS Back Porch(Blanking)	tvbp		16		TH	
VS Front Porch	tvfp	-	16	-	TH	

6.0 Reliability test items

Test Item	Test Conditions	Notes
High temperature Operation	Ta= +70℃, 96hrs	
Low temperature Operation	Ta= -20℃, 96hrs	
High Temperature Storage	Ta= +80℃, 96hrs	
Low Temperature Storage	Ta= -30℃, 96hrs	
Humidity Test	60℃ ,Humidity 90% ,96hrs	
Thermal Shock Test	-20℃,30min ~ +70℃,30min (30 cycle)	
Vibration Test(Packing)	Sine Wave 1.04G, 5~500Hz, XYZ 30min/each direction	

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7.0 INTERFACE PIN CONNECTION

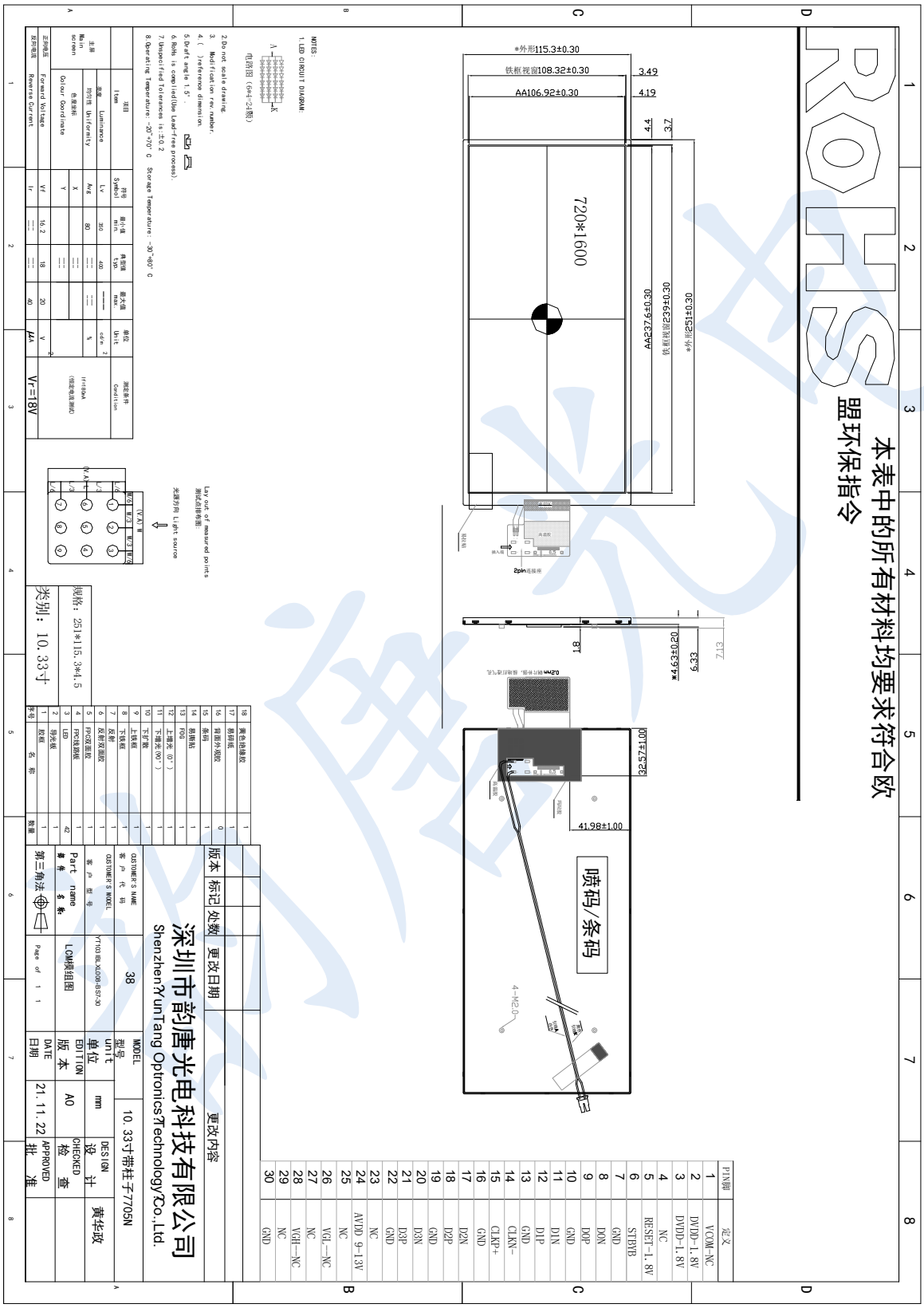
Signal of interface

Terminal No.	Symbol	I/O	Functions
1	VCOM	P	Common voltage（NC）
2	DVDD	P	Power for Digital Circuit（1.8V）
3	DVDD	P	Power for Digital Circuit（1.8V）
4	NC	O	No connection
5	RESET	P	Global reset pin. Active Low to enter Reset State. Normally pull high. Connecting with an RC reset circuit for stability（1.8V）
6	STBYB	I	Standby mode,normally pull high STBYB="1", normally operation STBYB="0", timing control,source driver will turn off（NC）
7	GND	P	Ground
8	MIPI_D0-	I	Negative MIPI differential data inputs0-
9	MIPI_D0+	I	Positive MIPI differential data inputs0+
10	GND	P	Ground
11	MIPI_D1-	I	Negative MIPI differential data inputs1-
12	MIPI_D1+	I	Positive MIPI differential data inputs1+
13	GND	P	Ground
14	MIPI_CLK-	I	Negative MIPI differential clock inputs
15	MIPI_CLK+	I	Positive MIPI differential clock inputs
16	GND	P	Ground
17	MIPI_D2-	I	Negative MIPI differential data inputs2-
18	MIPI_D2+	I	Positive MIPI differential data inputs2+
19	GND	P	Ground
20	MIPI_D3-	I	Negative MIPI differential data inputs3-
21	MIPI_D3+	I	Positive MIPI differential data inputs3+
22	GND	P	Ground
23	NC	O	No connection
24	AVDD	P	Power for Analog Circuit（9-13V）
25	NC	O	No connection
26	VGL	P	Gate OFF Voltage（NC）
27	NC	O	No connection
28	VGH	P	Gate ON Voltage（NC）
29	NC	O	No connection
30	GND	P	Ground

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8.0 OUTLINE DIMENSION



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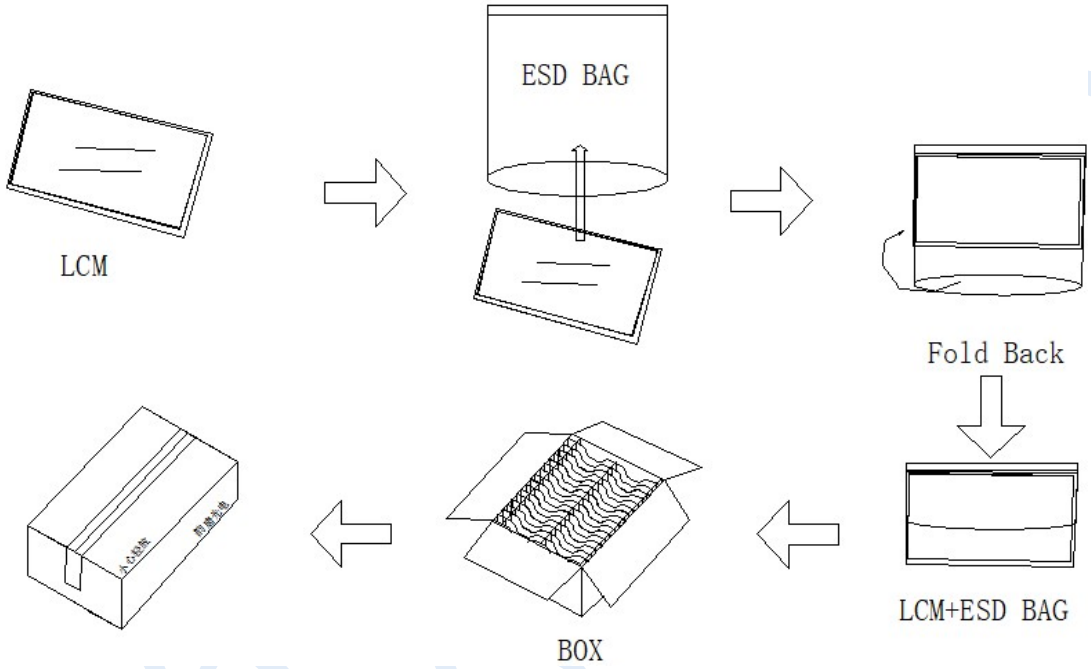
韵唐光电

9.0 Pakcage Specification

9.1 Packing form

LCM Moudle	LCM Qty. in the box	Box size	Note
YT103IBLXL008-BS7-30	20 pcs/box		

9.2 Packing assembly drawing



	Material	Notice
Box	Corrugated Paper Board	(AB Flute)
Partition/Pad	Corrugated Paper Board	(B Flute)
Corner Pad	Corrugated Paper Board	(AB Flute)
ESD bag	PE	

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10.0 General precaution

10.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

10.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. YT does not warrant the module, if customers disassemble or modify the module.

10.3 Breakage of LCD Panel

10.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

10.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

10.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

10.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

10.4 Electric Shock

10.4.1. Disconnect power supply before handling LCD module.

10.4.2. Do not pull or fold the LED cable.

10.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

10.5 Absolute Maximum Ratings and Power Protection Circuit

10.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

10.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

10.5.3. It's recommended to employ protection circuit for power supply.

10.6 Operation

10.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

10.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

10.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

10.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

10.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

10.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

10.8 Static Electricity

10.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

10.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

10.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

10.10 Disposal

When disposing LCD module, obey the local environmental regulations.

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